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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/964,586	FRUTSCHY ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,63 and 65-90* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,63,65-76,80-83 and 87-89* is/are rejected.

7)☒ Claim(s) *77-79,84-86 and 90* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *17*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosure Statement filed on 06-01-04 has been considered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4-7, 9, 64-66, 68, 70, 74,75, 82 and 83 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dibene, II et al. (US Pat. 6452113) in view of Dibene, II et al. (US Pat. 6452804).

Regarding claim 1, Dibene, II et al. ('113 patent) disclose a power module (see 600 in Fig. 6A/6B) having integrated circuits (IC)/an IC package comprising:

- a substrate (702 of an assembly 700 in Fig. 9 and 7) supporting the microprocessor/IC die (310 in Fig. 7; Col. 8, line 66) on the IC die of the substrate
- the power module (600/602 in Fig. 6A-9) comprising a packaged circuit board (PCB)/package frame (602 in Fig. 6A/6B and 9; Col. 8) mounted/attached at a peripheral area and above a perimeter of the substrate (see Fig. 9 and Fig. 7;

Col. 4, lines 25-28; Col. 8, lines 60-68; Col. 9, line 25) and arranged on the die-side of the substrate apart from the IC die on the substrate, and

- the power module providing a low impedance, low inductance power/current path to the die through the circuit components and electrical connectors (see 608A/608B and 612A/612B respectively in Fig. 6A/6B); and being functional as a power/ground impedance deliverer (PGID) to provide power/ground impedance delivery path/circuit (Col. 7, line 53- Col. 9, line 37)

(Fig. 6A-12; Col. 7, line 50- Col 10, line 25).

Dibene, II et al. ('113 patent) further teach the electrical connections/structure providing dual functions including a mechanical and electrical functions where the mechanical function includes the conductive interconnects providing a coupling/rigidity/support for the substrate (Col. 8, lines 50-60) and mechanical fasteners (802 in Fig. 9) proving the predetermined level of mechanical fastening/stiffening (Col. 9, lines 32-37).

Dibene, II et al. ('113 patent) further teach a variety of module assembly configurations including an embodiment where the package frame (see 2204 in Fig. 22) is positioned/mounted/attached at a peripheral/corner area including a perimeter of the substrate and extends along the perimeter and two side edges of the substrate (see 2204 and 2202 in Fig. 22; Fig. 22-25; Col. 14, line 16- Col. 15, line 22).

Dibene II, et al. ('113 patent) fail to explicitly teach the PCB/package frame being a package stiffener.

Dibene, II et al. ('113 patent) further teach another embodiment of Fig. 12, where an entire assembly including the PCB/package frame and a motherboard/stiffener board provides further support and stiffening for the components of the assembly (Col. 10, lines 8-25) such that the PCB/package frame and the motherboard/stiffener board function as the package stiffening components.

Dibene, II et al. ('804 patent) teach an integrated circuit (IC) package having an interposer substrate (104 in Fig. 1) supporting the microprocessor/IC die (101 in Fig. 1) where a power regulator PCB/electrical conductor assembly (102/103 in Fig. 1) delivering a low inductance current provides a mechanical/fastening support to the interposer substrate through non-compressible mechanical stand-offs/conductors (103 in Fig. 1; Col. 5, line 25; Col. 5, lines 25- 55). An entire assembly of the power regulator PCB/electrical conductor and a motherboard provides further support and stiffening for the components of the assembly such that the power regulator PCB and the motherboard function as the package stiffening components for the three-dimensional Integrated architecture/configuration (Col. 5, line 53- Col. 7, line 25).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the package stiffener concurrently providing a stiffening support as taught by the embodiment of Fig. 12 in Dibene, II et al. ('113

patent) and Dibene, II et al. ('804 patent) so that the mechanical coupling and the component support can be improved in Dibene, II et al's ('113 patent) package.

Regarding claims 4-6, Dibene II, et al. ('113 and '804 patents) teach substantially the entire structure as applied to claim 1 above, wherein Dibene II et al. ('113 patent) teach the substrate being a core substrate having a multiple internal layers in the IC- printed circuit board (IC-PCB) carrier package, the package having a variety of configurations including the flip chip ball grid/array device, built-up multiplayer (BML), pinned grid array- PGA and ceramic land grid array (CLGA), etc. (Col. 9, lines 10-30; Col. 7, lines 25- 43).

Regarding claim 7, Dibene II, et al. ('113 and '804 patents) teach substantially the entire claimed structure as applied to the claim 1 above, wherein Dibene II et al. ('113 patent) further teach the PCB/package frame being made of an electrically conductive surfaces/sections using conventional circuit board fabrication processing including etching and metallization (Col. 8, lines 24-37) to withstand conditions/temperature of normal IC operation (Col. 3, 4 and 7-16), but Dibene II et al. ('113 and 804 patents) fail to teach using the frame being made of one of a stamped, etched, extruded and deposited frame.

Regarding claim 7, Making or depositing the frame do not distinguish over Dibene II et al. ('113 and '804 patents) regardless of the process for forming the frame, because only the final product is relevant, not the process of making such as "molding/stamping/etching, etc. or laminating ". Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marrosi et al., 218 USPQ 289, all of which make it clear that it is the patentability and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not . Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Regarding claim 9, Dibene II, et al. ('113 and '804 patents) teach substantially the entire claimed structure as applied to the claim 1 above, wherein Dibene II et al. ('113 patent) further teach a heat sink/heat spreader plate assembly (1006/1010/1004 in Fig. 10-11B) being bonded to/supported on the PCB/package frame (Col. 9, line 40-67).

Regarding claims 63, 65 and 68, Dibene II, et al. ('113 and '804 patents) teach substantially the entire claimed structure as applied to the claim 1 above, wherein

Dibene II et al. ('113 patent) teach the package frame being configured to be functional as the PGID for the module and being in a form of a ring having a central aperture (604 in Fig. 6A/6B; Col. 8, line 26).

Regarding claims 64, 74 and 75, Dibene II, et al. ('113 and '804 patents) teach substantially the entire claimed structure as applied to the claim 63 above, wherein Dibene II et al. ('113 patent) further teach a heat sink/heat spreader plate/assembly (1006/1010/1004 in Fig. 10-11B) being integrally bonded to/coupled/supported on the package frame/PGID (Col. 9, line 40-67) such that the package frame/PGID and the IC die are in between the spreader plate and the substrate (see 602, 1006/1004, 302 and 702 respectively in Fig. 6A-11B).

Regarding claim 66, Dibene II, et al. ('113 and '804 patents) teach substantially the entire claimed structure as applied to the claim 63 above, wherein Dibene II et al. ('113 patent) further teach another embodiment (Fig. 14) where the package frame/PGID comprises two separate components/sections (see 1402 and 1404 in Fig. 14) being positioned on the respective section of the substrate (Col. 10, lines 35- Col. 11), the corner edges of the sections having rounded corners.

Regarding claim 70, Dibene II, et al. ('113 and '804 patents) teach substantially the entire claimed structure as applied to the claim 63 above, wherein Dibene II et al. ('113

patent) teach the package frame/PGID and the substrate being made of conventional circuit board material comprising insulating material/portions and metallized components/circuit layers (Col. 8, line 6; Col. 9, line 10), the package frame/PGID and the substrate having similar thermal properties such as coefficient of thermal expansion (CTE).

Regarding claims 82 and 83, Dibene II, et al. ('113 and '804 patents) teach substantially the entire claimed structure as applied to the claim 1 above, wherein Dibene II et al. ('113 patent) further teach another embodiment (Fig. 14) having the package frame/PGID comprising rectangular rounded shape with rounded corners (see 1402 and 1404 in Fig. 14; Col. 10, lines 35- Col. 11).

4. Claims 76 and 89 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dibene, II et al. ('113 and 804 patents) as applied to claim 1 above, and further in view of Belady (US Pat. 6285550).

Regarding claims 76 and 89, Dibene II, et al. ('113 and '804 patents) teach substantially the entire claimed structure as applied to the claim 1 above, except a power pod/plurality of power pods supplying the power to the IC die.

It is conventional in chip packaging and power supply/interconnect technology art to one or more power supply sources or power pods connecting various connectors and

components in a power module. Belady teaches a power module having a variety of electrical components including a substrate, microprocessor/die, heat sink, etc. where power supply is arranged through a conventional power pod (Col. 9, lines 17-23; Col. 8-10).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the power pod/pods supplying the power to the IC die as taught by Belady so that the desired flexibility in power supply arrangement can be achieved in Dehaine et al. and Dibene, II et al's ('113 and 804 patents) package.

5. Claims 2, 3, 67, 69, 71-73, 80, 81, 87 and 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dibene, II et al. ('113 and '804 patents) as applied to claims 1 and 63 above, and further in view of Dehaine et al. (US Pat. 5925925).

Regarding claim 2, Dibene, II et al. ('113 and '804 patents) teach substantially the entire claimed structure as applied to claims 1 and 63 above, except the stiffener including a copper (Cu) ring split into power and ground portions having an insulating couplers electrically isolating the power and ground portions of the Cu ring.

Dibene, II et al. ('113 patent) further teach the PCB/package frame comprising:

- plated through-holes and electrically conductive surfaces/pads (610, 616A/B respectively in Fig. 6A/B; Col. 8, lines 25-50) being electrically connected to a

conductive interconnect spacer having electrically conductive portions (612A/612B in Fig. 6A), the conductive layer/plating being copper (Cu)

- the conductive interconnect spacer providing dual functions including a mechanical support/coupling with the substrate and two separate conductive paths 616A and 616B in Fig. 6A/6B) including a first power path and a second ground path respectively in a coaxial arrangement (Col. 8, lines 50-68), and
- the electrically conductive portions of the conductive interconnect spacer being separated by an insulating dielectric portion/section (612 C in Fig. 6A; Col. 8, lines 37-47).

Dibene, II et al. ('113 patent) further teach in another embodiments of Fig. 13 and 14, a configuration of the power and ground conductive paths being provided in two concentric metal rings electrically isolated from each other (see 1306/1304 and 1404/1402 respectively in Fig. 13 and 14; Col. 10, lines 35- Col. 11, line 15) or using a plurality of two piece coaxial conductive interconnects at the corners of the IC die (Col. 9, lines 1-4).

Dehaine et al. teach a BGA package comprising a frame and a heat dissipating support plate (13 and 17 respectively in Fig. 1 and 3A/3C) where the frame is divided/split into four rings/sections of conductive planes (Q1-Q4 in Fig. 3A/3C) such that each ring/section is separated from each other by an insulating strip (23 in Fig.

3A/3C; Col. 10, line 57) and each ring/section can be electrically connected to different signal potentials/functions such as ground, desired voltage, etc. (see a ground ring 24 in Fig. 3A; Col. 11, line 9) in order to achieve the desired signal transmission and power decoupling functions (Col. 10, line 52- Col. 11, line 18).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the stiffener including a copper (Cu) ring split into power and ground portions having an insulating couplers electrically isolating the power and ground portions of the Cu as taught by the embodiments of Fig. 13 and 14 in Dibene, II et al. ('113 patent) and Dehaine et al. so that the desired ground/voltage routing and mechanical coupling can be achieved and the signal noise/interference can be reduced in Dibene, II et al's ('113 and '804 patents) package.

Regarding claim 3, Dibene, II et al. ('113 and '804 patents) teach substantially the entire claimed structure as applied to claims 1 and 2 above, wherein Dibene, II et al. further teach the conductive surfaces/paths being bonded/mounted on the substrate via conventional solder bonding to provide a low resistance/high current path and to remove heat from the substrate (Col. 10, lines 20-26; Col. 11, lines 9-15).

Regarding claims 67 and 69, Dibene II, et al. ('113 and '804 patents) teach substantially the entire claimed structure as applied to the claims 63 and 68 above, except the PGID

being positioned at separate corner edges of the substrate or having rounded corners respectively.

Dibene II et al. ('113 patent) further teach another embodiment (Fig. 14) where the package frame/PGID comprises two separate components/sections including corner edges (see 1402 and 1404 in Fig. 14) being positioned on the respective section of the substrate (Col. 10, lines 35- Col. 11), the corner edges having rounded corners.

Dehaine et al. teach the BGA package comprising a frame and a heat dissipating support plate (13 and 17 respectively in Fig. 1 and 3A/3C) where the frame is divided/split into four rings/sections of conductive planes (Q1-Q4 in Fig. 3A/3C) such that each ring/section being positioned at separate corner edges of a substrate.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the PGID being positioned at separate corner edges of the substrate or having rounded corners as taught by the embodiments of Fig. 13 and 14 in Dibene, II et al. ('113 patent) and Dehaine et al. so that the desired ground/voltage routing and mechanical coupling can be achieved and the signal noise/interference can be reduced in Dibene, II et al's ('113 and '804 patents) package.

Regarding claims 71-73, 80, 81, 87 and 88, Dibene, II et al. ('113 and '804 patents) teach substantially the entire claimed structure as applied to claims 1 and 63 above, except the PGID having a ground side and power side portions and having insulating couplers separating the power and ground portions and providing an aid in the structural integrity of the PGID.

Dibene, II et al. ('113 patent) further teach the package frame/PGID comprising:

- plated through-holes and electrically conductive surfaces/pads (610, 616A/B respectively in Fig. 6A/B; Col. 8, lines 25-50) being electrically connected to a conductive interconnect spacer having electrically conductive portions (612A/612B in Fig. 6A), the conductive layer/plating being copper (Cu)
- the conductive interconnect spacer providing dual functions including a mechanical support/coupling with the substrate and two separate conductive paths 616A and 616B in Fig. 6A/6B) including a first power path and a second ground path respectively in a coaxial arrangement (Col. 8, lines 50-68), and
- the electrically conductive portions of the conductive interconnect spacer being separated by an insulating dielectric portion/coupling section (612 C in Fig. 6A; Col. 8, lines 37-47).

Dibene, II et al. ('113 patent) further teach in another embodiments of Fig. 13 and 14, the PGID configuration comprising power and ground conductive paths being provided in two concentric metal rings electrically isolated from each other (see

1306/1304 and 1404/1402 respectively in Fig. 13 and 14; Col. 10, lines 35- Col. 11, line 15) and being bonded/soldered to provide an integral structure providing the desired power/ground paths from the die to the substrate.

Dehaine et al. teach a BGA package comprising a frame and a heat dissipating support plate (13 and 17 respectively in Fig. 1 and 3A/3C) where the frame is divided/split into four rings/sections of conductive planes (Q1-Q4 in Fig. 3A/3C) such that each ring/section is separated from each other by an insulating strip/coupling section (23 in Fig. 3A/3C; Col. 10, line 57), such configuration providing a structural integrity for the frame. Furthermore, each ring/section can be electrically connected to different signal potentials/functions such as ground, desired voltage, etc. (see a ground ring 24 in Fig. 3A; Col. 11, line 9) in order to achieve the desired signal transmission and power decoupling functions (Col. 10, line 52- Col. 11, line 18).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the PGID having a ground side and power side portions and having insulating couplers separating the power and ground portions and providing an aid in the structural integrity of the PGID as taught by the embodiments of Fig. 13 and 14 in Dibene, II et al. ('113 patent) and Dehaine et al. so that the desired ground/voltage routing and mechanical coupling can be achieved and the signal noise/interference can be reduced in Dibene, II et al's ('113 and '804 patents) package.

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dibene, II et al. ('113 and 804 patents) as applied to claims 1 and 2 above, and further in view of Dehaine et al. (US Pat. 5925925) and Banks et al. (US Pat. 6015722).

Regarding claim 8, Dibene II et al. ('113 and 804 patents) and Dehaine et al. teach substantially the entire claimed structure as applied to the claims 1 and 2 above, except using a thermal interface material and an epoxy to bond the heat spreader plate to the split copper ring and the die respectively.

Dibene II et al. ('113 patents) further teach a heat sink/heat spreader plate assembly (1006/1010/1004 in Fig. 10-11B) being bonded to the PCB/package frame and the IC die using a thermal interface material such as a thermal grease (Col. 9, line 40-67).

Banks et al. teach a heat dissipative flip chip package where a lid/heat spreader plate is bonded to a copper ring/stiffener (532 and 522 in Fig. 9) using a conventional adhesive material such as an epoxy (538 in Fig. 9; Col. 28, line 2) to provide the desired adhesion and moisture protection (Col. 26, line 30- Col. 28, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the thermal interface material and the epoxy to bond the heat spreader plate to the split copper ring and the die respectively as taught by Banks et al. so that the adhesion and moisture protection can be improved in Dehaine et al. and Dibene, II et al's ('113 and 804 patents) package.

Response to Arguments

7. Applicant's arguments filed on 06-01-04 have been fully considered but they are not persuasive.

A. Applicant contends that Dibene, II et al. patent or the combination ('113 and 804 patents) do not teach the PCB/package frame being the package stiffener and concurrently providing the stiffening support.

However, as explained above, Dibene, II et al. ('113 patent) teach the package frame structure providing dual functions including mechanical and electrical functions where the mechanical functions includes the conductive interconnects providing a coupling/rigidity/support for the substrate (Col. 8, lines 50-60) and mechanical fasteners (802 in Fig. 9) proving the predetermined level of mechanical fastening/stiffening (Col. 9, lines 32-37). Dibene, II et al. further teach another embodiment/invention (see Fig. 12 in '113 patent and Fig. 1 in '804 patent) where the entire assemblies including the PCB/package frame and a motherboard/stiffener board provides further support and stiffening for the components of the assembly such that the PCB/package frame and the motherboard or the stiffener board function as the package stiffening components.

Allowable Subject Matter

8. Claims 77-79, 84-86 and 90 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for Allowance

9. The following is an examiner's statement of reasons for allowance:

The references of record do not teach either singularly or in combination at least the limitations "the package stiffener includes a plurality of cooling fins" or "the package stiffener includes a capacitor", or "the PGID includes a plurality of cooling fins" or "the PGID includes a capacitor" in an integrated circuit (IC) package having a substrate where a power/ground/impedance deliverer (PGID) is disposed upon the die-side of the substrate and being spaced from the die to deliver low-inductance current to the die while concurrently providing stiffening support to the substrate.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NP

08-17-04

NITIN PAREKH

PATENT EXAMINER

TECHNOLOGY CENTER 2800